MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2022/2023

EEE3196 – INTEGRATED VLSI SYSTEMS

(EE)

12 JULY 2023
9.00 a.m – 11.00 a.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This examination paper consists of 7 pages with 4 questions only.
2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.

Formulas:

Ideal diode equation: $I_D = I_S(e^{\frac{V_D}{\phi_T}} - 1)$

$$V_T = V_{TO} + \gamma(\sqrt{|-2\emptyset_F + V_{SB}|} - \sqrt{|-2\emptyset_F|})$$

saturation:

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

linear:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right)$$

unified model:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DSAT} - \frac{{V_{DSAT}}^2}{2}\right)(1 + \lambda V_{DS})$$

$$t_P = \frac{C_L\frac{V_{SWING}}{2}}{I_{AVG}}$$

$$t_P = 0.69\,R_{eq}C_L$$

$$P_{dyn} = C_L{V_{DD}}^2 f$$

Question 1

(a) A Voltage Transfer Characteristics (VTC) graph for a CMOS inverter is shown in Figure Q1 (a) below.

(i) Redraw the VTC graph and label the critical voltages, lowest input voltage V_{IL}, highest input voltage V_{IH}, lowest output voltage V_{OL} and highest output voltage V_{OH} on the graph. [4 marks]

(ii) From part (i), calculate the high noise margin NM_H and low noise margin NM_L for the CMOS inverter. [2 marks]

(iii) In the VTC graph, state the operating modes for both PMOS and NMOS transistors on the dotted parts in the graph. The operating modes include saturation, linear and cutoff. [5 marks]

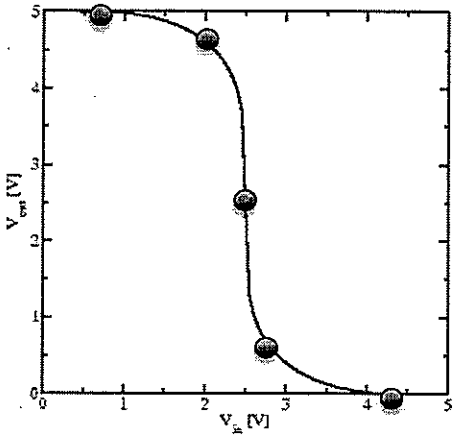

Figure Q1(a)

(b) Given a CMOS inverter with the following parameters:
$k'_n = 110\ \mu A/V^2$, $k'_p = -30\ \mu A/V^2$, $V_{Tn} = |V_{Tp}| = 0.4$ V, $V_{DD} = 3$ V, $V_{GS} = 2.7$ V, $(W/L)n = 2$, $(W/L)p = 5$ and $C_L = 20$ pF.

(i) Calculate the current (I_d) for the NMOS transistor when it is operating at saturation region with output voltage $V_{out} = 3$ V and linear region with output voltage $V_{out} = 1.5$ V respectively. [4 marks]

(ii) Using the average on-resistance (R_{on}) method, find the high-to-low propagation delay (t_{pHL}). [4 marks]

(iii) Using the average current (I_{avg}) method, find the high-to-low propagation delay (t_{PHL}). [4 marks]

(iv) Compare the answers for two different methods in Q1 (b) (ii) and Q1 (b) (iii) above and comment. [2 marks]

Continued...

Question 2

(a) Consider a uniform polysilicon wire with a length of 180 μm by 40 μm. Assume its sheet resistance value is 70 mΩ/square and the wiring capacitance values are given in Table Q2.

(i) Calculate the total lumped resistance of this wire. [2 marks]

(ii) Calculate the total capacitance associated with this wire. [6 marks]

(iii) Replace the polysilicon wire with a metal (Al2) wire. Calculate the total capacitance associated with this wire. [6 marks]

(iv) Based on total capacitance calculated from part (ii) and (iii) above, compare and comment on the preferred wire for interwire connection. [2 marks]

Table Q2

	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88			1st row: parallel plate in aF/μm² 2nd row: fringe in aF/μm			
	54						
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	

(b) Crosstalk in electronic circuits is a phenomenon that usually occurred due to undesired capacitive, inductive or conductive coupling from one circuit to another.

(i) Explain how capacitive crosstalk can happen in VLSI system. [3 marks]

(ii) Recommend THREE ways to reduce capacitive crosstalk. [6 marks]

Continued...

Question 3

(a) Given the following function:

$$F = (\overline{A.B}) + C$$

(i) Design and sketch the circuit using minimum conventional static CMOS transistors. [8 marks]

(ii) From part (i), modify the circuit using dynamic logic. [4 marks]

(iii) Describe the difference between static and dynamic logic. [2 marks]

(iv) There are also issues in dynamic logic. Describe at least TWO of the issues. [2 marks]

(b) Figure Q3(a) and Q3(b) show a dynamic sequential circuit and the clock signal inserted into the circuit, respectively.

(i) Describe the operation of the circuit when the CLK is low and $\overline{CLK}$ is high, and when the CLK is high and $\overline{CLK}$ is low. [5 marks]

(ii) If the CLK and $\overline{CLK}$ are overlapping each other, what will happen to the circuit? Suggest a method to fix it. [4 marks]

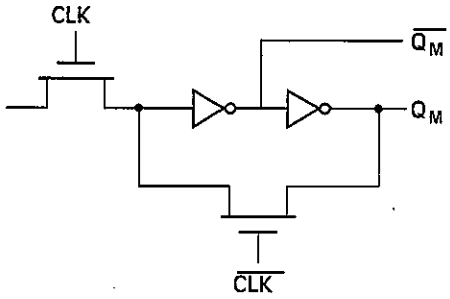

Figure Q3(a)

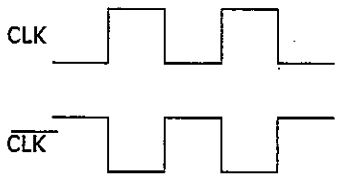

Figure Q3(b)

Continued...

Question 4

(a) Figure Q4(a) shows the cross section of a Flash EEPROM transistor. These transistors are used vastly in building NOR Flash memory as shown in Figure Q4(b) and Q4(c).

(i) Describe the operation of this Flash EEPROM transistor. [4 marks]

(ii) Based on Figure Q4(b), elaborate on the operation of this memory cell when it erases. [4 marks]

(iii) Based on Figure Q4(c), elaborate on the operation of this memory cell when it writes "1". [4 marks]

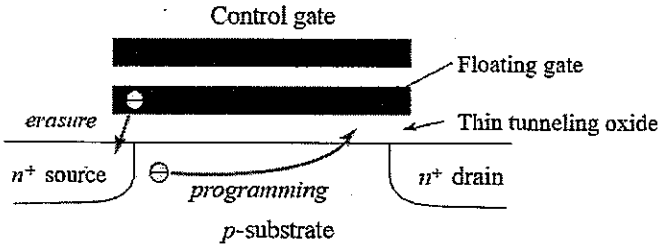

Figure Q4(a)

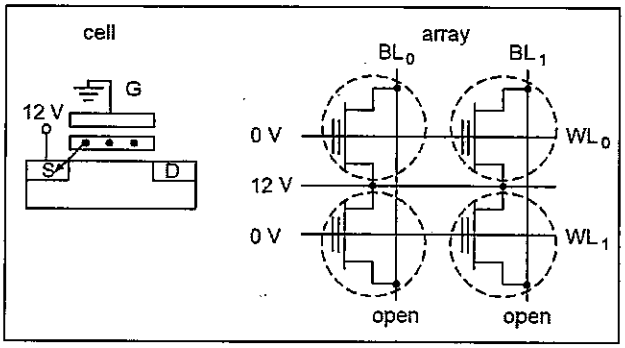

Figure Q4(b)

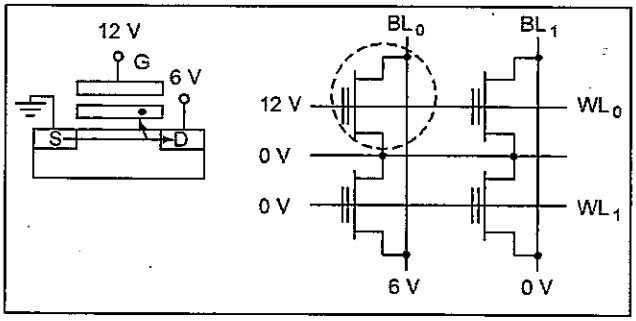

Figure Q4(c)

Continued...

(b) Given a 8-bit ripple carry adder (RCA) with different delays as listed below:
$t_{carry0\rightarrow1} = 200$ ps, $t_{carry1\rightarrow0} = 220$ ps,
$t_{sum0\rightarrow1} = 300$ ps, $t_{sum1\rightarrow0} = 320$ ps.

(i) Find the worst case delay t_{adder}. [3 marks]

(ii) Give an example of input values that will trigger this worst case delay. [2 marks]

(c) Figure Q4(d) shows the variation of power consumption of a 4-bit array multiplier using mirror full adder versus applied operational voltage at different technological nodes.

(i) Comment on the graph emphasizing on the power consumption. [4 marks]

(ii) Based on the graph, predict the propagation delay for the same 4-bit array multiplier as the applied operational voltage increases. Justify your reason for it. [4 marks]

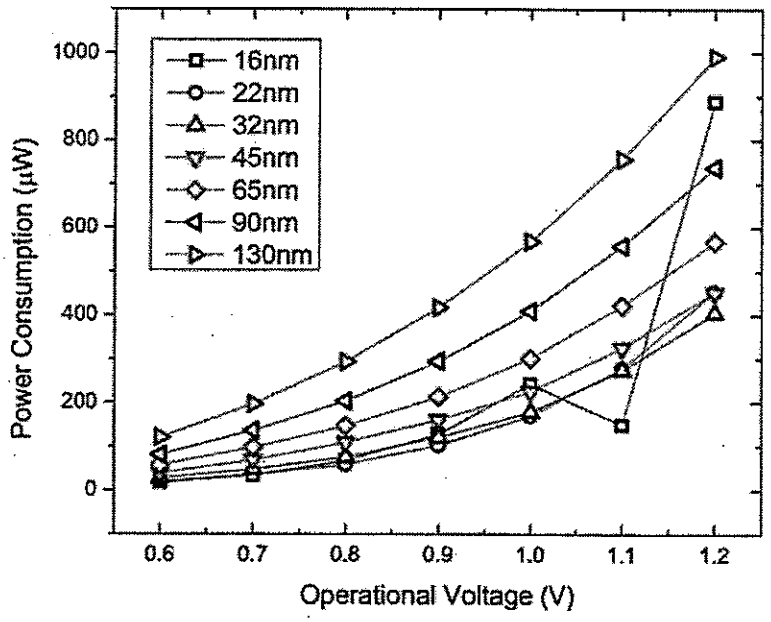

Figure Q4(d)

End of Paper